UNITED STATES PATENT AND TRADEMARK OFFICE

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/798,276	03/12/2004	Masami Hiramatsu	ASA-1174	6453

24956 7590 09/19/2006	EXAMINER
MATTINGLY, STANGER, MALUR & BRUNDIDGE, P.C. 1800 DIAGONAL ROAD SUITE 370 ALEXANDRIA, VA 22314	IQBAL, NADEEM

ART UNIT	PAPER NUMBER
2114	

DATE MAILED: 09/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

	Application No.	Applicant(s)
Office Action Summary	10/798,276	HIRAMATSU ET AL.
	Examiner	Art Unit	
	Nadeem Iqbal	2114	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE <u>3</u> MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 March 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-9* is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-9* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☒ All b)☐ Some * c)☐ None of:

    1.☒ Certified copies of the priority documents have been received.

    2.☐ Certified copies of the priority documents have been received in Application No. _____.

    3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☒ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *Mar 12, 04*.

4)☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.

5)☐ Notice of Informal Patent Application

6)☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

2.   This application currently names joint inventors. In considering patentability of the

claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various

claims was commonly owned at the time any inventions covered therein were made absent any

evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

the inventor and invention dates of each claim that was not commonly owned at the time a later

invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c)

and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

3.   Claims 1 & 5 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schwarm et

al., (U.S. Patent number 7028218) in view of Hashemi (U.S. Patent number 5491787).

4.   Schwarm et al., teaches (col. 2, lines 33-36) a redundant file server including at least first

processor and a second processor, the second processor board is programmed to assume the file

server functions of the first processor upon failure of the first processor. He also teaches (col. 9,

lines 62-64) that the first logical CPU of the first processor executes storage system microcode

under Microsoft NT operating system, and the second logical CPU of the processor executes

control station microcode under the Linux operating system. He thus teaches limitations pertain

to a first OS the first OS to conduct ordinary business processing and a second OS differing from

the first OS and an analysis and prediction application operating on the second OS. He does not

explicitly discloses first OS holds state information and that the analysis and prediction

application analyzes contents of information held by the first OS detecting sign of a failure.

Hashemi teaches (col. 3, lines 49-53) a fault tolerant system in which one processor is utilized

for operational purposes and the other processor would be used for checking operation of the

first processor for error or fault detection. It would have been obvious to a person of ordinary

skill in the art at the time the invention was made to include Hashemi invention into the

invention of Schwarm to be able to check operations of the first processor for error or fault

detection. This is because both invention are in the same environment of fault tolerance and

inclusion of Hashemi clearly provides a desirable advantage of checking operations of the first

processor and Schwarm teaches (col. 10, lines 39-41) microcode functions include control station

fail-over, and data mover failover, therefore provides motivation for the stated inclusion.

5.   Claims 2-4, 6-9 are rejected under 35 U.S.C. 103(a) as being unpatentable over Schwarm

et al., (U.S. Patent number 7028218) in view of Hashemi (U.S. Patent number 5491787) as

applied to claim 1 above, and further in view of Yasuda (U.S. Patent number 7069473).

6.   As per claim 2, Hashemi teaches (col. 5, lines 35-38) error reporting/handling module

which would receive and respond to any error indication produced by processors. Schwarm does

not explicitly discloses an auxiliary program that conducts processing against a failure of the first

OS. Yasuda teaches (col. 2, lines 49-51) a storage section for storing and holding fault recovery

information including rules for defining recovery operations when fault occurs in the at least one

computer system. It would have been obvious to a person of ordinary skill in the art to include

into the invention of Schwarm a storage section for storing and holding fault recovery

information including rules. This is because such an inclusion provides a desirable advantage for

recovering automatically from a fault and a fault monitoring apparatus as taught by Yasuda

teaches (col. 2, lines 45-47).

7.   As per claim 3, With reference to notification to an external terminal of contents of an

analyzed failure sign. Yasuda teaches at (col. 21, lines 52-54).

8.   As per claims 4 & 6, Schwarm et al., teaches (col. 9, lines 62-64) that the first logical

CPU of the first processor executes storage system microcode under Microsoft NT operating

system, and the second logical CPU of the processor executes control station microcode under

the Linux operating system. He thus teaches limitations pertain to a first OS the first OS to

conduct ordinary business processing and a second OS differing from the first OS and an

analysis and prediction application operating on the second OS. He does not explicitly discloses

first OS holds state information and that the analysis and prediction application analyzes contents

of information held by the first OS detecting sign of a failure. Hashemi teaches (col. 3, lines 49-

53) a fault tolerant system in which one processor is utilized for operational purposes and the

other processor would be used for checking operation of the first processor for error or fault

detection. He also teaches (col. 3, lines 53-55) a controller that would switch the processors

between normal and shadow operation. It would have been obvious to a person of ordinary skill

in the art to include Hashemi invention into the invention of Schwarm to be able to check

operations of the first processor for error or fault detection. This is because both invention are in

the same environment of fault tolerance and inclusion of Hashemi clearly provides a desirable

advantage of checking operations of the first processor and Schwarm teaches (col. 10, lines 39-

41) microcode functions include control station fail-over, and data mover failover, therefore

provides motivation for the stated inclusion.

9.   As per claim 7, With reference to notification to other virtual multi-OS sets of analyzed

contents. Yasuda teaches at (col. 21, lines 52-54). Hashemi also teaches (col. 3, lines 60-63).

10.   As per claim 8, Schwarm et al., teaches (col. 9, lines 62-64) that the first logical CPU of

the first processor executes storage system microcode under Microsoft NT operating system, and

the second logical CPU of the processor executes control station microcode under the Linux

operating system. He thus teaches limitations pertain to a first OS the first OS to conduct

ordinary business processing and a second OS differing from the first OS and an analysis and

prediction application operating on the second OS. He does not explicitly discloses analyzing

contents of state information and that the analysis and prediction application analyzes contents of

information held by the first OS detecting sign of a failure. Hashemi teaches (col. 3, lines 49-53)

a fault tolerant system in which one processor is utilized for operational purposes and the other

processor would be used for checking operation of the first processor for error or fault detection.

He also teaches (col. 3, lines 53-55) a controller that would switch the processors between

normal and shadow operation. It would have been obvious to a person of ordinary skill in the art

to include Hashemi invention into the invention of Schwarm to be able to check operations of the

first processor for error or fault detection. This is because both invention are in the same

environment of fault tolerance and inclusion of Hashemi clearly provides a desirable advantage

of checking operations of the first processor and Schwarm teaches (col. 10, lines 39-41)

microcode functions include control station fail-over, and data mover failover, therefore provides

motivation for the stated inclusion.

11.   As per claim 9, Hashemi teaches (col. 5, lines 35-38) error reporting/handling module

which would receive and respond to any error indication produced by processors. Schwarm does

not explicitly discloses an auxiliary program that conducts processing against a failure of the first

OS. Yasuda teaches (col. 2, lines 49-51) a storage section for storing and holding fault recovery

information including rules for defining recovery operations when fault occurs in the at least one

computer system. It would have been obvious to a person of ordinary skill in the art to include

into the invention of Schwarm a storage section for storing and holding fault recovery

information including rules. This is because such an inclusion provides a desirable advantage for

recovering automatically from a fault and a fault monitoring apparatus as taught by Yasuda

teaches (col. 2, lines 45-47).

Conclusion

Any inquiry concerning this communication or earlier communications from the

examiner should be directed to Nadeem Iqbal whose telephone number is (571)-272-3659. The

examiner can normally be reached on M-F (8:00-5:30) First Friday Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's

supervisor, Scott Baderman can be reached on (571)-272-3644. The fax phone number for the

organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent

Application Information Retrieval (PAIR) system. Status information for published applications

may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR

system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would

like assistance from a USPTO Customer Service Representative or access to the automated

information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Nadeem Iqbal
Primary Examiner
Art Unit 2114

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